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Wafer-scale laser pantography: Fabrication of *n*-metal-oxide-semiconductor transistors and small-scale integrated circuits by direct-write laser-induced pyrolytic reactions[a)]

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A complete set of processes sufficient for manufacture of *n*-metal-oxide-semiconductor (*n*-MOS) transistors by a laser-induced direct-write process has been demonstrated separately, and integrated to yield functional transistors. Gates and interconnects were fabricated of various combinations of *n*-doped and intrinsic polysilicon, tungsten, and tungsten silicide compounds. Both 0.1-μm and 1-μm-thick gate oxides were micromachined with and without etchant gas, and the exposed *p*-Si [100] substrate was cleaned and, at times, etched. Diffusion regions were doped by laser-induced pyrolytic decomposition of phosphine followed by laser annealing. Along with the successful manufacture of working *n*-MOS transistors and a set of elementary digital logic gates, this letter reports the successful use of several laser-induced surface reactions that have not been reported previously.

PACS numbers: 42.60.Kg, 81.15.Gh, 85.30.Tv, 85.40.Ci

Direct laser writing and processing semiconductor surfaces for electronic applications is becoming recognized as a versatile and powerful technology.[1] Lasers have been utilized to etch,[2,3] dope,[4,5] and deposit[6–9] materials on crystalline silicon substrates interfacing gaseous reactants. Both photolytic (gas phase photodissociation)[8] and pyrolytic (surface heating)[5] techniques have been used to demonstrate the submicrometer spatial resolution obtainable with direct laser writing. This letter reports the first fabrication of transistors using solely direct laser-write techniques ("laser pantography"). These *n*-metal-oxide-semiconductor (*n*-MOS) transistors and small-scale integrated circuits were made using several new, as well as some previously demonstrated, direct laser writing, pyrolytic methods. The fabrication cycle and preliminary results on early transistor and digital logic devices are reported here.

The experimental apparatus used in these studies is diagrammed in Fig. 1. A cw argon-ion laser (5145 Å) is amplitude modulated (with typically 20 ns–10 ms pulses) by an electro-optic switch positioned between cross-polarized Glan–Thompson prisms. Desired peak powers up to ~ 10 W are obtained by suitably rotating the $\lambda/2$ plate placed at the laser output and by applying the appropriate switching voltage on the electro-optic modulator. The temporally controlled laser beam is then imaged on the semiconductor substrate by a 6-cm focal length lens followed by a 28×, 0.45-N.A. microscope objective. At times, arc lamp light also irradiates the substrate through this objective and projects an image onto a vidicon through an eyepiece, in this expanded microscope arrangement, to support direct viewing of the surface or impinging laser beam. This magnified laser beam spot is also projected on an *x-y* scanning pinhole-photodiode assembly to permit spot size measurement of the focused beam. The typical focused beam spot diameter ($1/e$ intensity points) in these experiments was 1.9 μm.

The target wafer is mounted in a stainless steel chamber, topped with a sapphire entrance window, which is directly plumbed into the gas handling/vacuum system. This reaction chamber is mounted on a pair of 0.5-μm resolution *x-y* stepper motor-driven translation stages, which control the spatial position of the wafer. An LSI-11/23 microcomputer interface provided dynamic control of the incident laser pulse properties (intensity, pulse width, frequency, number of pulses per processing site, number of processing cycles) and also controlled motion of the *x-y* translation stage, to permit the programming of direct laser write processes over a wide variety of possible process parameters. The wafer is at ambient temperature during irradiation.

The target substrates were *p*-type [100], 3.4–4.6-Ω cm crystalline silicon with a predeposited, uniform silicon diox-

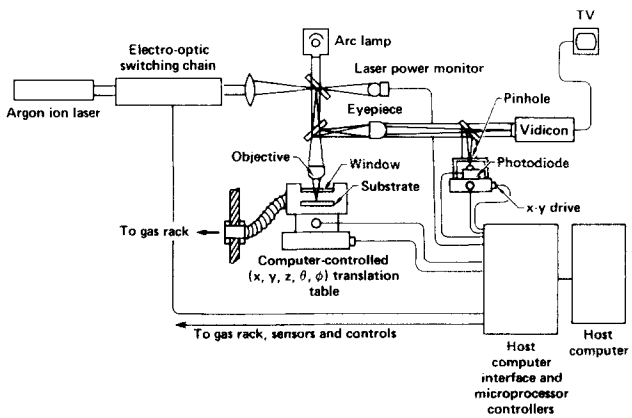

FIG. 1. Experimental setup for direct laser writing; see text for further details.

[a)] This is the third paper in the series; the previous paper, "Wafer-Scale Laser Pantography:II. Laser-Induced Pyrolytic Creation of MOS Structures," was delivered at the Conference on Lasers and Electro-Optics, Baltimore,Maryland, May, 1983, Lawrence Livermore National Laboratory UCRL-88537 (available NTIS).

ide film on the surface. To date, substrates with either 1 μm oxide grown by a wet thermal oxidation process or 900 Å oxide grown by a dry thermal oxidation process have been used to fabricate MOS field-effect transistors (MOSFET's). Before installation in the reaction chamber, the wafer is sequentially immersed in boiling solutions of trichloroethane, acetone, methanol, and de-ionized water in a clean room environment. The wafer is then mounted in the reaction chamber, and baked out under high vacuum. The final surface preparation step is *in situ* ozone etching; the ozone is produced by flowing oxygen through the reaction chamber while irradiating with UV radiation from a Hg arc lamp. This is followed by high vacuum bake out of the entire cell. Prior to introducing each new reagent gas for use in the reaction cell, the vessel is flushed several times with helium or nitrogen, and is then passivated with a sample of the new reactant. All reagents were used as supplied by the manufacturer without further purification, except for pumping off possible volatiles at 77 K as required.

The process developed for MOS transistor fabrication is diagrammed in Fig. 2. A conducting gate structure of dimension typically 1–5 μm wide and 10-30 μm long is first deposited on the oxide and "wired" to a probing pad. These pads are typically 30–40 μm squares that are made by the same process as the gate. Diffusion regions are patterned by removing the oxide in two rectangular regions ($\sim 30 \times 40$ μm) abutting either side of the gate. This is sometimes followed by etching the exposed silicon. Removing the oxide to make substrate electrical ground is also accomplished in this step. The source and drain are appropriately n-type doped with phosphorus, pulse-laser annealed, and then attached to probing pads. Device characteristics are currently measured after the wafer has been removed from the chamber.

Several alternate technologies have been tested for each step outlined above. These are briefly described here.

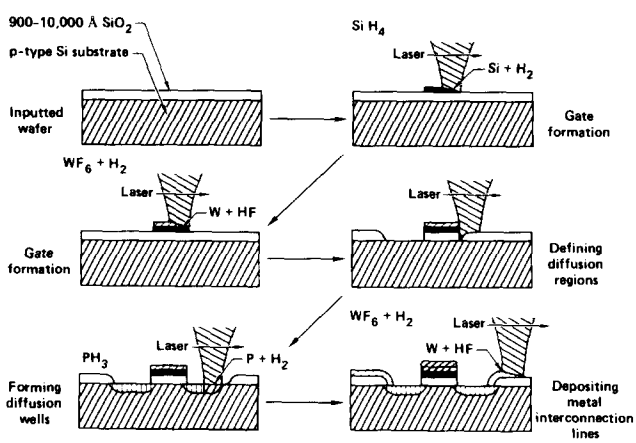

FIG. 2. Schematic of the steps involved in MOS transistor fabrication by laser pantography, as described in the text. After cleaning the inputted wafer (p-type Si with SiO_2 overlayer), gate structures are formed by depositing polysilicon and tungsten. The diffusion regions are defined by removing the oxide; the locally bare silicon substrate is cleaned and sometimes etched (not shown), and appropriately doped with phosphorus. Metal interconnection lines (and probing pads, as needed) are then deposited. To ensure electrical isolation, in a refined version of this last step currently under development, there are instead several repeated sequences of thick (> 1 μm) field oxide deposition, followed by oxide removal at the desired interconnect sites and deposition of metal interconnects.

For the gate structures and interconnects, doped and undoped polycrystalline silicon, tungsten, and tungsten silicides were examined. The most successful structures were formed by depositing polysilicon using a silane/disilane/phosphine mixture; this was sometimes followed by forming a tungsten overlayer. Typically, rapid deposition of highly localized features was accomplished by first irradiating with relatively high laser powers (0.5–1.0 W) to seed the surface, and then over-writing the deposits several times at lower laser powers to obtain the desired film thickness.

Silicon deposition was studied using various mixtures of silane,[6,7] disilane, and trisilane at 100–800 Torr, sometimes laced with phosphine (0.01–0.5%). The temperature thresholds for deposition decreased with increasing silane chain length, as predicted by the chemical vapor deposition experiments of Gau *et al.*[10] Disilane surface reactions produced deposits at laser powers as low as ~ 0.1 W (focused to 1.9-μm beam diameter). The rate of deposition was on the order of 0.5–5 mm/s, depending on laser power and gas pressure. Using trisilane, silicon features were deposited much faster than with disilane; however, they were much less localized.

Localization of the silicon deposits decreased with increasing laser power and increasing integrated irradiation times. The approximate deposition rate using silane was a factor of 2–5 below that of disilane (at similar pressures), but silane-deposited silicon was usually more localized. Polysilicon linewidths as narrow as 0.9 μm were deposited onto 0.1-μm-thick oxide by the silane reaction. Such enhanced localization (linewidths ~ 2.5 times smaller than the effective laser beam diameter) is predicted by theory.[11]

Doped silicon was deposited by adding small levels of phosphine (0.01–0.5% PH_3) to the 800 Torr silane. The relatively rapid surface deposition of phosphorus on the oxide apparently increased the nucleation barrier over that of undoped silicon, consistent with the observation of Everstyn and Put.[12] Lines with resistivities of $\sim 10^{-2}$–10^{-3} Ω cm were deposited in this fashion.

Tungsten lines were deposited on both silicon and silica by the laser-induced pyrolytic hydrogen reduction of tungsten hexafluoride.[9] Experiments were performed with a 3:1–4:1 ratio of hydrogen: tungsten hexafluoride, with the pres-

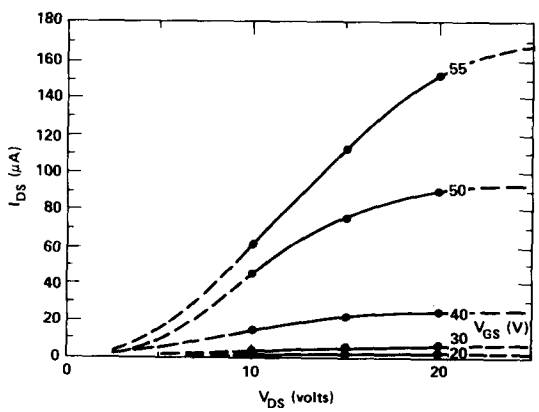

FIG. 3. dc I-V characteristics of a laser-fabricated n-MOSFET with 1-μm-thick gate oxide, with drain-source current plotted vs drain-source voltage for a sequence of gate-source biasing voltages.

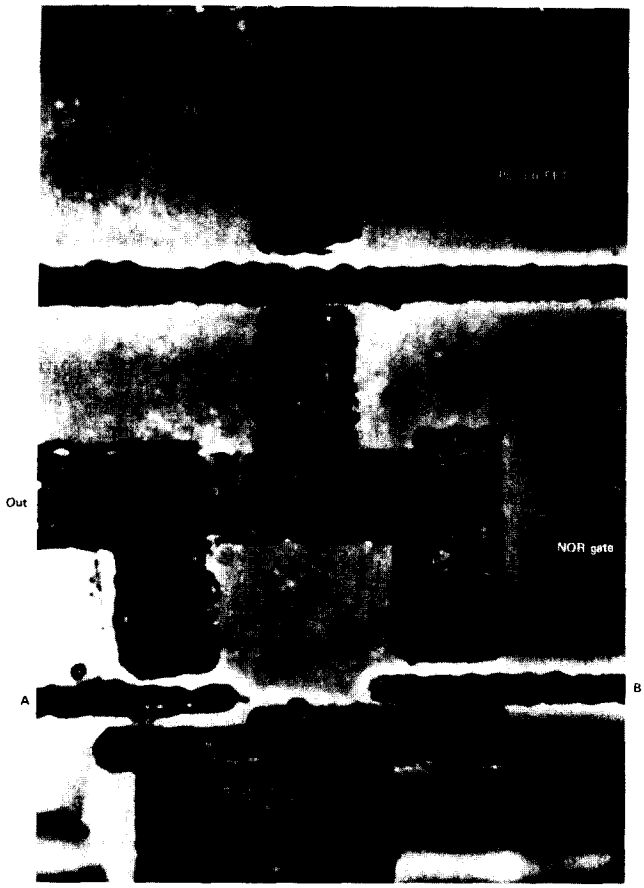

FIG. 4. Two-input NOR gate, fabricated with two parallel MOSFET's whose gates are the *A* and *B* inputs, whose sources are tied to ground and whose drains are tied together to a pull-up FET at the NOR output point.

sure totalling 800 Torr. This reaction proceeded at laser beam powers as low as ~ 0.1 W. When tungsten deposition was initiated with higher laser beam powers (0.6–0.8 W), using 1–10-μs pulses, the deposited material appeared shiny and metallic.

Silicon dioxide etching by local laser heating was examined in vacuum, H_2 and H_2-buffered HCl. Sufficiently rapid and localized oxide removal occurred by locally heating the oxide (by silicon substrate absorption followed by heat transfer to the surface) in vacuum, with an etch rate of ~ 40 μm/s for ~ 3.5 W incident laser power. No damage to the surrounding oxide was observed by optical means. The oxide removal mechanism may involve the known decomposition of SiO_2 on Si at temperatures above 900 °C to form the volatile SiO.[13] With use of 180 Torr HCl/540 Torr H_2 over the substrate, the etch rate was increased to ~ 100 μm/s with only 0.6 W incident beam power. After oxide removal, the exposed silicon substrate was either cleaned by laser heating (desorption) in vacuum or etched by pyrolytic reactions with H_2-buffered HCl.[2]

The source and drain regions of MOSFET's were doped by first either depositing a phosphorus surface layer (0.5 Torr PH_3/800 Torr He) or by laying down a thin layer of doped polysilicon (by surface pyrolyzing a PH_3/SiH_4 gas mixture). Afterwards, the dopants were driven in by annealing with 1–10-μs duration pulses of 1–2-W power. These intensity levels were sufficient to cause transient local melting, and changes in the color of the source and drain regions were observed which were attributed to recrystallization of previously amorphous silicon.

MOSFET devices were made with both 1-μm and 0.09-μm-thick gate oxides. The dc I–V properties of a 1-μm-thick gate oxide transistor are shown in Fig. 3. The ~ 30 V gate threshold is that predicted by theory for this thick gate oxide field-effect transistor. Gate thresholds for MOSFET's with 0.09-μm gate oxide thickness were in the 3–5-V range. The leakage current levels in these early devices significantly affected device performance at higher source-drain voltages.

Small sets of these MOSFET's have been interconnected to realize NOT, NOR, and NAND gates, the latter with two inputs each. One of these is shown in Fig. 4.

Studies are continuing to better characterize and control the different process steps for ultralarge scale integrated (ULSI) circuit prototyping via the mask-free, resist-free, direct laser writing approach described here. This technology allows complete fabrication, testing, and repair of ULSI circuits in a single environment. The system of Fig. 1 is presently being upgraded to support creation of ULSI circuits by extremely rapid ($\sim 10^3$/s) fabrication, interconnection, and testing of *n*-MOS transistors with submicron minimum feature sizes.

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[1] R. M. Osgood, Jr., Ann. Rev. Phys. Chem **34** (in press).
[2] D. J. Ehrlich, R. M. Osgood, Jr., and T. F. Deutsch, Appl. Phys. Lett. **38**, 1018 (1981).
[3] F. A. Houle and T. J. Chuang, J. Vac. Sci. Technol. **20**, 790 (1982).
[4] T. F. Deutsch, D. J. Ehrlich, D. D. Rathman, D. J. Silversmith, and R. M. Osgood, Jr., Appl. Phys. Lett. **39**, 825 (1981).
[5] D. J. Ehrlich and J. Y. Tsao, Appl. Phys. Lett. **41**, 297 (1982).
[6] D. J. Ehrlich, R. M. Osgood, Jr., and T. F. Deutsch, Appl. Phys. Lett. **39**, 957 (1981).
[7] D. Bauerle, P. Irsigler, G. Leyendecker, H. Noll, and D. Wagner, Appl. Phys. Lett. **40**, 819 (1982).
[8] D. J. Ehrlich, R. M. Osgood, Jr., and T. F. Deutsch, J. Vac. Sci. Technol. **21**, 23 (1982).
[9] S. D. Allen and A. B. Tringubo, J. Appl. Phys. **54**, 1641 (1983).
[10] S. C. Gau, B. R. Weinberger, M. Akhtar, Z. Kiss, and A. G. MacDiarmid, Appl. Phys. Lett. **39**, 436 (1981).
[11] I. P. Herman, R. A. Hyde, B. M. McWilliams, A. H. Weisberg, and L. L. Wood, Materials Research Society Symposia Proceedings (November 1982), **17**, *Laser Diagnostics and Photochemical Processing for Semiconductor Devices*, edited by R. M. Osgood, Jr., S. R. J. Brueck, and H. R. Schlossberg (Elsevier, New York, 1983), p.9.
[12] F. C. Eversteyn and B. H. Put, J. Electrochem. Soc. **120**, 106 (1973).
[13] J. C. Bean, in *Impurity Doping Processes in Silicon*, edited by F. F. Y. Wang (North-Holland, New York, 1981), p.189.